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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,065	06/20/2003	Ming-Huei Shieh	AF01169/AMDP975US	5651

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EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2178	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,065	SHIEH ET AL.	
	Examiner	Art Unit	
	Dang T Nguyen	2178	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to communications: Application filed on 06/20/2003.

2. Claims 1 - 27 are pending in this case. Claims 1, 13, 17, and 24 are independent claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 - 15, are 17 - 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Le et al. U.S. Patent No. US 6,690,602 B1 - filed Apr. 8, 2002.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding independent claim 1, Fig. 3 of Lee et al. discloses an architecture that facilitates a reference voltage in a multi-bit memory [302], comprising:

a multi-bit memory core [302] including a plurality of data cells [10]

for storing data; first a and second reference arrays [Dynamic Reference A, Dynamic Reference B] of a plurality of multi-bit reference cells [10's of Reference A, 10's of Reference B], the first and second reference arrays fabricated on the memory core (Fig. 3); and a first bit value of a first reference cell (Fig. 4 [414]) of the first reference array (Fig. 4 [Ref A]) averaged with a second bit value of a second reference cell (Fig. 4 [418]) of the second reference array (Fig. 4 [Ref B]) to arrive at the reference voltage (Fig. 4 (A+B)/2).

Regarding dependent claim 2, Fig. 3 of Le et al. further discloses comprising a sector [Sector 1] of multi-bit data cells [10] organized in rows and columns with associated word lines [WLs] attached to the multi-bit data cells [10] in a row and with associated bit lines [BLs] attached to the multi-bit data cells [10] in a column, the first and second reference cells [304, 306] forming a multi-bit reference pair (Fig. 4) that is programmed and erased with the multi-bit data cells [10] during programming and erase cycles (Col. 6 lines 7 - 21).

Regarding dependent claim 3, Fig. 3 of Le et al. discloses wherein the multi-bit reference pair [304, 306] is associated with a word in a word line [WL0], the multi-bit reference pair utilized during reading of bits of the word (Col. 4 lines 15 - 17).

Regarding dependent claim 4, Fig. 3 of Le et al. discloses wherein the multi-bit reference pair [304, 306] is associated with multi-bit data cells [10s] in a wordline [WL0], the multi-bit reference pair [304, 306] utilized during reading of bits in the wordline (Col. 4 lines 15 – 17).

Regarding dependent claim 5, Fig. 3 of Le et al. further discloses comprising a plurality of the multi-bit reference pairs [304,306] associated with and attached to a

corresponding word line (WL), the associated multi-bit reference pair [304, 306] utilized during reading of bits in the corresponding word line (Col. 4 lines 15 – 17).

Regarding dependent claim 6, Fig. 3 of Le et al. further discloses comprising the multi-bit reference pair [304,306] is associated with multi-bit data cells [10] in the sector (Sector 1), the multi-bit reference pair [304, 306] utilized during reading of bits in the sector (Col. 4 lines 15 – 17).

Regarding dependent claim 7, Le et al. discloses wherein the memory core (Fig. 3) including a plurality of data sectors (Col. 5 lines 40 - 42) that are accessible by the first and second reference arrays [304, 306], the first and second reference arrays [304, 306] located the plurality of data sectors (Fig. 3 disclosing multiple sectors separates by a broken lines for each sector, and the broken line on the right side of the Reference B clearly teaches there is at least one more sector which located on the right side of 304 and 306).

Regarding dependent claim 8, Figs. 1–3 of Le et al. discloses an integrated circuit comprising the memory.

Regarding dependent claim 9, Fig. 3 of Le et al. discloses a memory core of computer system.

Regarding dependent claim 10, Fig. 3 of Le et al. discloses an electronic device of memory system.

Regarding dependent claim 11, Le et al. discloses the first and second reference arrays (Fig. 3 [304, 306]) including corresponding reference cells (Fig. 4 [404, 406]) that are interleaved among the data cells (Fig. 4 [402]).

Regarding dependent claim 12, Fig. 3 of Le et al. discloses a plurality of data sectors (Col. 5 lines 40 - 42) such that each data sector is associated with at least one of the first and second reference array [304, 306] of multi-bit reference cells [10s].

Regarding independent claim 13, (Figs. 3 and 4) of Le et al. disclose an architecture that facilitates a reference voltage (Fig. 4) in a multi-bit memory comprising: a multi-bit memory core (Fig. 3) for storing data, the memory core including two groups (Col. 5 lines 40 – 42) of data sectors (Fig. 3 [10s]); first and second reference arrays (Fig. 3 [304, 306]) of a plurality of multi-bit reference cells (REFERENCE A, B), the first and second reference arrays (Fig. 3 [304, 306]) fabricated on the memory core (Fig. 3) interstitial to the groups (Col. 5 lines 40 – 42) of data sectors (Fig. 3 [10s]); a first bit value (Fig. 4 [404]) of a first reference cell (Fig. 3 [304]) of the first reference array (Fig. 3 [10s of 304]) and a second bit value (Fig. 4 [406]) of a second reference cell (Fig. 3 [306]) of the second reference array (Fig. 3 [10s of 306]) forming a reference pair whose respective bit values are averaged (Fig. 4 [(A+B)/2]) to arrive at the reference voltage.

Regarding dependent claim 14, Le et al discloses the groups (Col. 5 lines 40 – 42) of data sectors read in an interleaved manner with a selected reference pair (Fig. 4, Col. 4 lines 15 - 17).

Regarding dependent claim 15, Le et al. discloses wherein the first and second reference arrays precharged before being averaged (Fig. 4) and (Col. 3 lines 8-27).

Regarding independent claim 17, the claim incorporated substantially same subject matter as of claim 1, and is rejected along the same rationale.

Regarding dependent claim 18, the claim incorporated substantially same subject matter as of claim 2, and is rejected along the same rationale.

Regarding dependent claim 19, the claim incorporated substantially same subject matter as of claim 3, and is rejected along the same rationale.

Regarding dependent claim 20, the claim incorporated substantially same subject matter as of claim 4, and is rejected along the same rationale.

Regarding dependent claim 21, the claim incorporated substantially same subject matter as of claim 5, and is rejected along the same rationale.

Regarding dependent claim 22, the claim incorporated substantially same subject matter as of claim 6, and is rejected along the same rationale.

Regarding dependent claim 23, the claim incorporated substantially same subject matter as of claim 7, and is rejected along the same rationale.

Regarding independent claim 24, the claim incorporated substantially same subject matter as of claim 1, and is rejected along the same rationale.

Regarding dependent claim 25, the claim incorporated substantially same subject matter as of claim 11, and is rejected along the same rationale.

Regarding dependent claim 26, the claim incorporated substantially same subject matter as of claim 2, and is rejected along the same rationale.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16 and 27 are rejected under 35 U.S.C. 103(a) as being obvious over Le et al. ('602') in view of Le et al. U.S. Patent No. 6,643,177 B1 – filed Jan. 21, 2003.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding dependent claims 16 and 27, Lee et al. (US'602') as applied to claims 1 and 24 above disclosed every aspect of applicant's claimed invention except for a redundancy array located at least one of proximate and adjacent to the groups of data sectors.

Fig. 2 of Lee et al. (US '177') discloses a redundancy array (225) located at least one of proximate and adjacent to the groups of data sectors.

Lee et al. '602' and '177' are the same inventors and same subject matter of reference voltage for read in a flash memory device. Therefore it would be obvious for Lee et al. or one ordinary skill in the art at the time the invention was made to incorporated the redundancy device taught by Lee et al. '177' into Lee et al. '602' for the purpose of serving as an duplicate for preventing failure of memory device.

Prior art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Khalid et al.	Patent No. US 6,538,922 B1	Date of Patent: Mar. 25, 2003
Bill et al.	Patent No. 5,754,475	Date of Patent: May. 19, 1998
Fong	Patent No. 5,537,358	Date of Patent: Jun. 16, 1996
Sweha et al.	Patent No. 5,497,354	Date of Patent: Mar. 5, 1996

Contact Information

6. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (703) 305-1673. Normal contact times are M-F, 8-4:30.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Heather Herndon, may be reached at (703) 308-5186.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 746-7239 (for formal communications intended for entry)

or:

(703) 746-7238 (for after-final communications)

Hand-delivered responses should be brought to

Crystal Park II, 2121 Crystal Drive

Arlington, VA, Fourth Floor (receptionist).

Dang Nguyen 6/23/2004

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